United States Patent [19]

Wincn et al.

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[54] **SAMPLING COMPARATOR CIRCUIT FOR PROCESSING A DIFFERENTIAL INPUT**

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[52] **U.S. Cl.** **307/494**; 307/493; 307/497; 307/291; 328/206; 330/112; 330/260

[58] **Field of Search** ..... 307/493, 494, 497, 498, 307/501, 350, 530, 352, 353, 247 R, 279, 291; 328/195, 206; 330/112, 260

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[57] **ABSTRACT**

An MOS sampling comparator circuit including a differential amplifier for producing first and second amplified signals, a first positive feedback circuit for further amplifying the first amplified signal, a second positive feedback circuit for further amplifying the second amplified signal, a strobed latch, having a positive feedback circuit, for further amplifying and storing the signals from the first and second positive feedback circuits, and a circuit for outputting complementary logic signals in response to the latched signals. By providing the first and second positive feedback circuits, small analog differential voltage input signals to the differential amplifier are further amplified and coupled without delay to the latch, resulting in an accurate conversion of the analog input signals to logic signals at high speed.

11 Claims, 2 Drawing Figures